EECE 352 Computer Architecture

Course Syllabus, Spring 2013

Course Description

It is important for both computer hardware and software developers to understand the interactions between the computer's architecture and its software. This course introduces the organizational paradigms that determine the capabilities and performance of computer systems. The topics we will cover includes: Register transfer level machine organization; MIPS instruction set architecture; performance metrics; computer arithmetic; organization and detailed implementation of non-pipelined and pipelined processors; cache and virtual memory; introduction to parallel/multicore processors.

Textbook:

[1]. "Computer Organization & Design - The Hardware and Software Interface" Revised 4th edition, by David A. Patterson and John L. Hennesy, (ISBN: 978-0-12-374750-1), published Nov. 2011.

Prerequisites:

EECE 351.

Class Times:

Tuesday & Thursday, 10:05am ~ 11:30am

Class Location:

SSW-321

Instructor Info.:

Dr. Yu Chen
Office: ES-2309,
Phone: (607) 777 - 6133,
Email: ychen@binghamton.edu
Office Hour: 3:00 ~ 4:00pm, Tuesday & Thursday, or by appointment.

Grading:

✓ Assignments	30% (5% x 6)
✓ Project	25% (5% + 10% + 10%)
✓ Exams	45% (20% + 25%)

Policies:

The university academic integrity code is listed in the University Bulletin. Category I violations will result in a grade of **ZERO** for the work plus a one letter course grade reduction. Category II violation will result in a failing grade of the course. (http://bulletin.binghamton.edu/integrity.htm)